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| Terms | Documents |
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| key with address | 21815 |

**Database:** US Pre-Grant Publication Full-Text Database; US Patents Full-Text Database; US OCR Full-Text Database; EPO Abstracts Database; JPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

**Search:** L14

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## Search History

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| Set Name side by side | Query | Hit Count | Set Name result set |
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| *DB=PGPB,USPT,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR* | | | |
| L14 | key with address | 21815 | L14 |
| L13 | l3 with L12 | 82 | L13 |
| L12 | l4 with processor | 2050 | L12 |
| *DB=USPT; PLUR=YES; OP=OR* | | | |
| L11 | partition$ adj2 processor | 511 | L11 |
| L10 | l6 | 34 | L10 |
| L9 | l4 | 15898 | L9 |
| *DB=PGPB,USPT,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR* | | | |
| L8 | l5 and l6 | 13 | L8 |
| L7 | l2 with l5 | 416 | L7 |
| L6 | l2 with l4 | 74 | L6 |
| L5 | partition$ | 411042 | L5 |
| L4 | memory adj2 (map or table) | 25508 | L4 |
| L3 | rout$ | 753516 | L3 |
| L2 | router | 60951 | L2 |
| L1 | 6247109.pn. | 2 | L1 |

END OF SEARCH HISTORY

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You may refine your search by editing the current search expression or entering a new one in the text box.

router <and> memory <and> mapping Search

☐ Check to search within this result set

**Results Key:**
**JNL** = Journal or Magazine **CNF** = Conference **STD** = Standard

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1 **An architecture based on the memory mapped node addressing in reconfigurable interconnection network**
*Ikedo, T.; Yamada, J.; Nonoyama, Y.; Kimura, J.; Yoshida, M.;*
Parallel Algorithms/Architecture Synthesis, 1997. Proceedings. Second Aizu International Symposium , 17-21 March 1997
Pages:50 - 57

[Abstract] [PDF Full-Text (816 KB)] **IEEE CNF**

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2 **A scalable cache coherent scheme exploiting wormhole routing networks**
*Yunseok Rhee; Joonwon Lee;*
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Pages:223 - 226

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3 **EMPOWER: a cluster architecture supporting network emulation**
*Pei Zheng; Ni, L.M.;*
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Pages:617 - 629

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4 **A high-performance architecture and BDD-based synthesis methodology for packet classification**
*Prakash, A.; Kotla, R.; Mandal, T.; Aziz, A.;*
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 22 , Issue: 6 , June 2003
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8 **Performance analysis of multi-dimensional packet classification on programmable network processors**
*Srinivasan, D.; Wu-chang Feng;*
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9 **High-performance IP routing table lookup using CPU caching**
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10 **Incremental routing in FPGAs**
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11 **FPGA-based Internet Protocol Version 6 router**
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[Abstract] [PDF Full-Text (64 KB)] **IEEE CNF**

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12 **An empirical study of datapath, memory hierarchy, and network in SIMD array architectures**

*Herbordt, M.C.; Weems, C.C.;*
Computer Design: VLSI in Computers and Processors, 1995. ICCD '95.
Proceedings., 1995 IEEE International Conference on , 2-4 Oct. 1995
Pages:546 - 551